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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,277	07/23/2003	Dong-Sauk Kim	29926/39495	8394

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EXAMINER	
TRAN, THANH Y	
ART UNIT	PAPER NUMBER
2822	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/625,277	KIM ET AL.	
	Examiner	Art Unit	
	Thanh Y. Tran	2822	

The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-11,13-17 and 19-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-11,13-17 and 19-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 7-8, 11, 14-16, 19-21, 24-27 and 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Durcan et al (U.S. 6,395,600).

As to claim 7, Durcan et al discloses in figures 1 and 6B a semiconductor device, comprising: a plurality of capacitor plugs ("contact site" 5) formed within a predetermined interval interleaved between two bit lines ("a bit line-to-bit line", see col. 1, lines 38-47; or "adjacent bit lines", see col. 8, lines 50-60) and midpoints of capacitor plugs (5) are located at inter-section points of X axis virtual line and Y axis virtual line, wherein the X axis virtual lines are parallel with the bit lines and the Y axis virtual lines are perpendicular to the X axis virtual lines (see figures 1 and 6B, the X axis can be the line of plugs 5 in horizontal direction, and the Y axis can be the line of plugs 5 in vertical direction); a plurality of lower electrodes ("bottom electrode" 20) of capacitors formed within a predetermined interval to be respectively connected with the capacitor plugs (5) in one to one correspondence, each lower electrode ("bottom electrode" 20) being circularly shaped; and a plurality of contact pads (1) formed between the lower electrodes (20) and the capacitor plugs (5), wherein the contact pads (1) are formed over

the capacitor plugs (5) (see figure 6B) and disposed at a lower plane of at least one of the paired lower electrodes (20).

As to claim 8, Durcan et al discloses in figures 1 and 6B a semiconductor device, wherein a midpoint of the contact pad (1) is located at an upper plane of the capacitor plug (5) along one of two X virtual axes (the X axes can be the lines of plugs 5 in horizontal direction) which is adjacent to each other.

As to claim 11, Durcan et al discloses in figures 1 and 6B a semiconductor device, wherein size of the upper plane of the contact pad (1) is greater than that of the upper plane of the capacitor plug (5).

As to claim 19, Durcan et al discloses in figures 1 and 6A-6B a semiconductor device and a corresponding method for fabricating a semiconductor device, comprising: forming a plurality of capacitor plugs ("contact site" 5) within a predetermined interval interleaved between two bit lines ("a bit line-to-bit line", see col. 1, lines 38-47; or "adjacent bit lines", see col. 8, lines 50-60) by arranging midpoints of capacitor plugs ("contact site" 5) located at inter-section points of X axis virtual line and Y axis virtual line, wherein the X axis virtual lines are parallel with the bit lines and the Y axis virtual lines are perpendicular to the X axis virtual lines (see figures 1 and 6B, the X axis can be the line of plugs 5 in horizontal direction, and the Y axis can be the line of plugs 5 in vertical direction); forming a plurality of lower electrodes ("bottom electrode" 20) of capacitors within a predetermined interval to be respectively connected with the capacitor plugs ("contact sites" 5) in one to one correspondence, each lower electrode ("bottom electrode" 20) being circularly shaped; wherein a plurality of contact pads (1) are respectively formed between the lower electrodes ("bottom electrode" 20) and the capacitor plugs ("contact site" 5) after

forming the capacitor plugs (5) (figure 6B), wherein the contact pads (1) serve as connecting the lower electrode (20) with the capacitor plug (5) electrically.

As to claim 20, Durcan et al discloses in figures 1 and 6A-6B a semiconductor device and a corresponding method for fabricating a semiconductor device, wherein the contact pads (1) are formed over the capacitor plugs ("contact site" 5) and midpoints of the contact pads (1) are located at a lower plane of at least one of the paired lower electrodes ("bottom electrode" 20) along the X virtual axis (see figure 6B).

As to claim 21, Durcan et al discloses in figures 1 and 6A-6B a semiconductor device and a corresponding method for fabricating a semiconductor device, wherein the contact pads (1) are disposed on upper planes of the capacitor plugs ("contact site" 5) of which midpoints are located along one of a pair of X virtual axes adjacent to each other (see figure 6B, X virtual axes are an axes in horizontal direction).

As to claim 24, Durcan et al discloses in figures 1 and 6A-6B a semiconductor device and a corresponding method for fabricating a semiconductor device, wherein size of the upper plane of the contact pad (1) is greater than that of the upper plane of the capacitor plug ("contact site" 5).

As to claim 25, Durcan et al discloses in figures 1 and 6A-6B a semiconductor device and a corresponding method for fabricating a semiconductor device, wherein a lower electrode ("bottom electrode" 20) and neighbored lower electrode (neighbored "bottom electrode" 20) disposed along a direction of Y virtual axis line (vertical direction) are formed not to have overlapped area or to have minimum overlapped are if one of lower electrode (20) is moved to same X virtual axis line (horizontal direction) of the other lower electrode (20).

As to claim 26, Durcan et al discloses in figures 1 and 6A-6B a semiconductor device and a corresponding method for fabricating a semiconductor device, wherein a lower electrode ("bottom electrode" 20) and neighbored lower electrode (neighbored "bottom electrode" 20) disposed along a direction of Y virtual axis (vertical direction) are not on same Y virtual axis (vertical direction).

As to claim 27, Durcan et al discloses in figures 1 and 6A-6B a semiconductor device and a corresponding method for fabricating a semiconductor device, wherein the midpoints of a lower electrode (20) and the neighbored lower electrode (neighbored 20) are not disposed along same Y virtual axis (vertical direction).

As to claim 29, Durcan et al discloses in figures 1 and 6A-6B a semiconductor device and a corresponding method for fabricating a semiconductor device, wherein an area of an upper plane of a lower electrode (20) is practically identical to that of a lower plane of the lower electrode (20) in view of a three-dimensional structure and the lower electrode features a circular cylinder structure having a lateral plane connecting the upper plane with the lower plane, wherein the lateral plane is practically vertical to the upper plane and lower plane respectively (upper plane/lower plane can be an upper surface/lower surface of 20).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 9-10, 22-23, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Durcan et al (U.S. 6,395,600).

As to claims 9 and 22, Durcan et al does not disclose a midpoint of the contact pad is deviated from the midpoint of a corresponding capacitor plug but located at a midpoint of the corresponding lower electrode. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor device of Durcan et al by rearrange the position of the contact pad so that the midpoint of contact pad is located at a midpoint of the corresponding lower electrode for providing a conductive extension for the lower electrode of the semiconductor device, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

As to claim 10, Durcan et al discloses in figures 1 and 6B a semiconductor device, wherein the lower electrode (20) corresponding to the contact pad (1) and another lower electrode (20) which is adjacent to the lower electrode (20) corresponding to the contact pad (1) along the Y virtual axis (see figure 1, contact pads 1 are along the Y axis – vertical direction) are disposed at positions deviated from the Y virtual axis in an opposite direction (lower electrodes 20 are in the X axis –horizontal direction that is in an opposite direction with the Y virtual axis).

Durcan et al does not disclose a midpoint of the contact pad is located at a midpoint of the corresponding lower electrode. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor device of Durcan et al by rearrange the position of the contact pad so that the midpoint of contact pad is located at a midpoint of the corresponding lower electrode for providing a conductive extension for the lower

electrode of the semiconductor device, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

As to claim 28, Durcan et al does not disclose a ratio of a major axis to a minor axis of the upper plane of the lower electrodes ranges from about 1 to 1 to about 2 to 1. However, *a ratio of a major axis to a minor axis of the upper plane of the lower electrodes ranges from about 1 to 1 to about 2 to 1* would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

As to claim 23, Durcan et al discloses in figures 1 and 6A-6B a semiconductor device and a corresponding method for fabricating a semiconductor device, wherein the lower electrode ("bottom electrode" 20) corresponding to the contact pad (1) and an adjacent lower electrode (20) found along the Y virtual axis are disposed in a way crossing each other (see figures 6A-6B).

Durcan et al does not disclose a midpoint of the contact pad is located at a midpoint of the corresponding lower electrode. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the semiconductor device of Durcan et al

by rearrange the position of the contact pad so that the midpoint of contact pad is located at a midpoint of the corresponding lower electrode for providing a conductive extension for the lower electrode of the semiconductor device, since it has been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70.

5. Claims 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Durcan et al (U.S. 6,395,600) in view of Lee et al (U.S. 6,656,789).

As to claim 13, Durcan et al discloses in figures 1 and 6A-6B a semiconductor device and a corresponding method for fabricating a semiconductor device, comprising: forming a plurality of capacitor plugs ("contact site" 5) within a predetermined interval interleaved between two bit lines ("a bit line-to-bit line", see col. 1, lines 38-47; or "adjacent bit lines", see col. 8, lines 50-60) by arranging midpoints of capacitor plugs ("contact site" 5) located at inter-section points of X axis virtual line and Y axis virtual line, wherein the X axis virtual lines are parallel with the bit lines and the Y axis virtual lines are perpendicular to the X axis virtual lines (see figures 1 and 6B, the X axis can be the line of plugs 5 in horizontal direction, and the Y axis can be the line of plugs 5 in vertical direction); forming a plurality of lower electrodes ("bottom electrode" 20) of capacitors within a predetermined interval to be respectively connected with the capacitor plugs ("contact sites" 5) in one to one correspondence, each lower electrode ("bottom electrode" 20) being circularly shaped; wherein forming the plurality of lower electrodes ("bottom electrode" 20) comprises: depositing a sacrifice insulation layer ("masking layer" 99, figure 6A) over the capacitor plug ("contact sites" 5) formed over a semiconductor substrate (11); forming a plurality of open parts (see the open parts as shown in figure 6B that expose capacitor plugs 5) exposing

the capacitor plugs ("contact sites" 5) by performing an selective etching (62A) of the sacrifice insulation layer ("masking layer" 99) by using a mask pattern ("masking layer") (see figures 6A-6B); depositing a material (24, figure 6B) for the lower electrode ("bottom electrode" 20) on an entire profile of the semiconductor substrate (11) comprising the open parts (see the open parts as shown in figure 6B that expose capacitor plugs 5); forming the lower electrodes (20) separated from each other by performing a planerization process ("planar") until the sacrifice insulation layer (99) is exposed (see Fig. 6A, col. 8, lines 11-16); and removing the sacrifice insulation layer (99).

Durcan et al does not disclose the step of removing the sacrifice insulation layer by carrying out a wet dip-out process.

Lee et al teaches in figures 5-6 a semiconductor device and a corresponding method comprising a step of removing the sacrifice insulation layer (36) by carrying out a wet dip-out process ("a wet etch process") (see col. 7, lines 35-40). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the semiconductor device and the corresponding method of Durcan et al by using a wet dip-out process for removing the sacrifice insulation layer as taught by Lee et al for preventing the problem of the electric short between the bottom electrodes (lower electrodes). One skilled in the art would have been motivated because a wet dip-out process ("a wet etch process") is also an easy etch process.

As to claim 14, Durcan et al discloses in figures 1 and 6A-6B a semiconductor device and a corresponding method for fabricating a semiconductor device, wherein the mask pattern (mask pattern of 99, figure 6A) having an open part (see the open part as indicated at 1 in figure 6A)

and neighbored open part (see other open parts of elements 1 in figure 6B) disposed along a direction of the Y virtual axis line are formed not to have overlapped area if the open part is moved to the same X virtual axis line as the other open part.

As to claim 15, Durcan et al discloses in figures 1 and 6A-6B a semiconductor device and a corresponding method for fabricating a semiconductor device, wherein the mask pattern (mask pattern of 99, figure 6A) having the open part (see the open part as indicated at 1 in figure 6A) and neighbored open part (see other open parts of elements 1 in figure 6B) disposed along a direction of the Y virtual axis are not on the same Y virtual axis.

As to claim 16, Durcan et al discloses in figures 1 and 6A-6B a semiconductor device and a corresponding method for fabricating a semiconductor device, wherein the mask pattern (mask pattern of 99, figure 6A) having the open part (see the open part as indicated at 1 in figure 6A) and the neighbored open part (see other open parts of elements 1 in figure 6B) are not disposed along the same Y virtual axis.

As to claim 17, Durcan et al discloses in figures 1 and 6A-6B a semiconductor device and a corresponding method for fabricating a semiconductor device, wherein the open part (see the open part as indicated at 1 in figure 6A) of the mask pattern (mask pattern of 99) features an octagonal (see figure 6B).

Durcan et al in view of Lee et al does not disclose a ratio of a major axis to a minor axis of the open part ranges from about 1 to 1 to about 2 to 1. However, *a ratio of a major axis to a minor axis of the open part ranges from about 1 to 1 to about 2 to 1* would have been obvious to an ordinary artisan practicing the invention because, absent evidence of disclosure of criticality for the range giving unexpected results, it is not inventive to discover optimal or workable ranges

by routine experimentation. In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). Furthermore, the specification contains no disclosure of either the critical nature of the claimed dimensions of any unexpected results arising therefrom. Where patentability is aid to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. See In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Response to Arguments

6. Applicant's arguments filed 11/24/06 have been fully considered but they are not persuasive.

Applicant argued that Durcan does not disclose capacitor plugs formed within a predetermined interval interleaved between two bit lines.

In response, the examiner does not agree with applicant's argument because Durcan clearly teaches the memory array structure comprising two adjacent bit lines ("a bit line-to-bit line", see col. 1, lines 38-47; or "adjacent bit lines", see col. 8, lines 50-60), and the capacitor plugs ("contact sites" 5) are in the interleaved interval, as shown in figures 1 and 6B, and are formed within the structure having two adjacent bit lines, thus they are formed within a predetermined interval interleaved between two bit lines (see figures 1 and 6B, and "a bit line-to-bit line" in col. 1, lines 38-47; and "adjacent bit lines" in col. 8, lines 50-60).

Applicant further argued that Durcan does not disclose contact pads formed between the lower electrodes and the capacitor plugs.

In response, the examiner does not agree with applicant's argument because Durcan clearly teaches contact pads (1) formed between the lower electrodes (20) and the capacitor plugs

(5) (see figure 6B). See figure 6B of Durcan, there is at least a portion of contact (1) is formed between the lower electrodes (20) and the capacitor plugs (5).

Applicant further argued that Durcan et al fails to disclose contact pads are disposed at a lower plane of at least one of the paired lower electrodes.

In response, the examiner does not agree with applicant's argument because Durcan clearly teaches in figure 6B that contact pads (1) are disposed at a lower plane of at least one of the paired lower electrodes (20). A upper surface of the lower electrode (20) (as shown in figure 6B) can be considered as a lower surface or lower plane of the lower electrode (20) if the structure of Durcan, as shown in figure 6B, is capable of turning up side down. Thus, Durcan clearly disclose in figure 6B that contact pads (1) are disposed at a lower plane (lower surface) of at least one of the paired lower electrodes (20).

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (571) 272-2110. The examiner can normally be reached on M-F (9-6:30pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith, can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TYT

Zandra V. Smith
Supervisory Patent Examiner
19 March 2007